REMARKS

Claims 1-93 were previously pending in the application. Claims 1, 9, 18, 24, 31, 33, 37, 41, 52, 54, 61, 66, 81-83, 85-90 and 92 are amended herein. Claims 15, 84, 91 and 93 are cancelled herein without prejudice. The Examiner is respectfully requested to reconsider and withdraw the rejection(s) in view of the amendments and remarks contained herein.

Applicants have renumbered claims 66-92 to 67-93 per the Examiner's request. Various informalities in Claims 24, 31 and 66 were also corrected per the Examiner's request.

REJECTION UNDER 35 U.S.C. § 102

Claims 1-8, 10-13, 15-17, 23, 63-67, 69 and 78 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Nagakari et al. (U.S. Pat. No. 6,282,079). This rejection is respectfully traversed.

Claim 1 recites a capacitor that is adapted to be mounted to a substrate and that includes m electrode plates that are oriented perpendicular to the substrate when connected to the substrate. The capacitor has a height above the substrate that is greater than the width of the capacitor.

As best understood by Applicant, Nagakari et al. does not show, teach or suggest a capacitor having m electrode plates that are oriented perpendicular to a substrate. Nagakari et al. also does not show, teach or suggest a capacitor having a height above the substrate that is greater than the width.

The height of the capacitor above the substrate in Nagakari et al. is less than the width which may be due to the orientation of the electrodes. In Nagakari et al., the electrode or plates of the capacitors are oriented parallel to an underlying substrate. See Nagakari et al, FIGs. 3-4, 22-23. The parallel orientation of the electrodes or plates in Nagakari et al. causes the capacitor to take up more valuable real estate on the printed circuit board or other substrate, which increases the cost of the system. Furthermore, there is no teaching or suggestion in Nagakari et al. to adjust the orientation of the electrodes relative to the underlying substrate.

Therefore, Applicant believes that Claim 1 is allowable over Nagakari et al.

Claims 24, 41, 60, 85, 88, and 91 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Ahiko et al. (U.S. Pat. No. 6,292,351). This rejection is respectfully traversed.

Claims 24 recites a capacitor structure that includes a second capacitor that is mounted on the first capacitor.

As best understood by Applicant, Ahiko et al. does not show, teach or suggest mounting a first capacitor on a second capacitor. Ahiko et al. mounts the capacitors on a printed circuit board. None of the embodiments show, teach or suggest mounting one capacitor on another capacitor as set forth in Claim 24. The first embodiment in FIGs. 1-4 of Ahiko et al. is mounted to a PCB. External sides are supplied with supply voltages. See col. 7, line 44 to col. 8, line 32. The second, third and fourth embodiments in FIGs. 5-8, 9-12 and 13-16 also show attachment to PCBs.

Claim 41 recites a capacitor structure that includes a second capacitor that is disposed adjacent to a first capacitor and that includes s third external terminals that are coupled to corresponding ones of said s second terminals of said first capacitor.

As set forth above, Ahiko et al. does not show, teach or suggest mounting a first capacitor adjacent to a second capacitor. Ahiko et al. mounts the capacitors on a printed circuit board and connects supply potentials. None of the embodiments in Ahiko et al. show, teach or suggest mounting one capacitor adjacent and in contact with another capacitor.

Therefore, Applicant believes that Claims 24 and 41 are allowable over Ahiko et al.

Claims 24, 26-29, 31-32, 34-37, 41-43, 45, 47-51, 53, 59, 70, 72-74 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kuroda et al. (U.S. Pat. No. 6,594,136). This rejection is respectfully traversed.

Claims 24 and 41 recite a capacitor structure that is adapted to be mounted on a substrate and that includes m electrode plates that are oriented perpendicular to the substrate when the n first external terminals are connected to the substrate. Claims 24 and 41 are also restricted to a capacitor structure that includes a second capacitor that is mounted on or adjacent to the first capacitor, respectively.

As best understood by Applicant, Kuroda et al. does not show, teach or suggest a capacitor having m electrode plates that are oriented perpendicular to a substrate. The capacitor plates of Kuroda et al. are oriented parallel to an underlying substrate. The parallel orientation of the electrode plates in Kuroda et al. requires the capacitor to

take up more valuable real estate on the printed circuit board or other substrate, which increases system cost.

Kuroda et al. also does not show, teach or suggest a capacitor structure including a second capacitor that is mounted on or adjacent to a first capacitor. Kuroda et al. mounts the capacitors on a printed circuit board as shown in FIGs. 17 and 18. None of the embodiments show, teach or suggest mounting one capacitor adjacent and in contact with another capacitor.

Therefore, Applicant believes that Claims 24 and 41 are allowable over Kuroda et al.

REJECTION UNDER 35 U.S.C. § 103

Claims 1, 23, 63, 81, 84 and 93 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ahiko et al. in view of Nagakari. This rejection is traversed.

Claim 1 recites a capacitor that includes m electrode plates that are oriented perpendicular to a substrate and that has a height above the substrate that is greater than the width of the capacitor.

As set forth above, Nagakari et al. does not show, teach or suggest a capacitor having m electrode plates that are oriented perpendicular to a substrate. Nagakari et al. also does not show, teach or suggest a capacitor having a height above the substrate that is greater than the width.

As set forth above, Ahiko et al. also does not show, teach or suggest a capacitor having a height above the substrate when mounted that is greater than the width.

Thus even if the references are properly combinable, they fail to show, teach or suggest all of recited limitations of Claim 1.

Applicant believes, however, that these references are not properly combinable. Nagakari et al. disclose a capacitance structure that has a reduced impedance that is achieved by orienting the electrode plates parallel to an underlying substrate and arranging terminals connected to the electrode plates around a periphery of the electrode plates to the substrate to achieve four capacitors in parallel. For example, see Col. 6, lines 37-55 and other similar sections. Therefore, it would not be consistent with Nagakari et al. to orient the electrode plates perpendicular to the substrate as in Ahiko et al. because the electrode plates would not be able to achieve the intended result.

Finally Ahiko et al. clearly describes a capacitor structure having a height above the substrate that is significantly less than the width.

Therefore, Applicants believe that Claim 1 is allowable over the proposed combination of Ahiko et al. and Nagakari et al.

Claims 1 and 9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Galvangi et al. (U.S. Patent No. 5,799,379) in view of DuPre et al. (U.S. Patent No. 6,243,253) and Nakagari et al.

At the outset, Applicant believes that the combination of Galvangi et al. with Nakagari et al. and/or DuPre et al. is improper. The Examiner admits that Galvangi et al. does not show, teach or suggest any of the elements of Claim 1 other than a capacitor. As set forth above, Nagakari et al. does not show, teach or suggest a capacitor having m electrode plates that are oriented perpendicular to a substrate. As

set forth above, Nagakari et al. also does not show, teach or suggest a capacitor having a height above the substrate that is greater than the width.

It is inconsistent with the teachings of Nagakari et al. to orient the electrode plates of the capacitor perpendicular to the substrate on which it is mounted since this would prevent the connection of the electrode plates as shown and taught by Nagakari et al. and as previously described above. The parallel orientation of the plates in Nagakari et al. is important to achieve the four capacitors in parallel. Thus, Applicants believe that Nagakari et al is not properly combinable with Galvangi et al. and or DuPre et al.

As best understood by Applicant, DuPre et al. does not show, teach or suggest a capacitor having m electrode plates that are oriented perpendicular to a substrate on which it is mounted. The electrodes of DuPre et al. are parallel to the substrate. See FIG.s 1-11B. While being consistent with the electrode orientation in Nakagari et al., it is not consistent with the claimed capacitor structure. Furthermore, this orientation occupies a significant amount of chip real estate, which increases system cost. As best understood by Applicant, DuPre et al. also does not show, teach or suggest a capacitor having a height above the substrate that is greater than the width as recited in the claims.

Therefore, Applicant believes that Claim 1 is allowable over the proposed combination of Nakagari et al., Galvangi et al. and DuPre et al.

Claims 24, 26-35 and 41-52 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Galvangi et al. (U.S. Patent No. 5,799,379) in view of DuPre et al. (U.S. Patent No. 6,243,253).

With respect to Claim 24, none of the references show, teach or suggest connecting even ones of m electrodes of a first capacitor to even first external terminals and odd ones of the m electrodes of the first capacitor to odd first external terminals where m is an integer greater than 3.

The Examiner admits that Galvangi et al. does not show, teach or suggest any of the elements of the claim other than interconnected first and second capacitors. Furthermore, each pad in Galvangi et al. is connected to only a single electrode as shown in FIG. 9. Having m greater than 3 requires each of the first external terminals to be connected to two or more electrode plates. Galvangi et al. does not show this arrangement.

As set forth above, DuPre et al. does not show, teach or suggest a capacitor having m electrode plates that are oriented perpendicular to a substrate on which it is mounted. The electrodes of DuPre et al. are parallel to the substrate. See FIG.s 1-11B. While being consistent with the electrode orientation in Nakagari et al., it is not consistent with the claimed capacitor structure. Furthermore, this orientation occupies a significant amount of chip real estate.

With respect to Claim 41, in addition to the claim recitations and arguments identified above with respect to Claim 24, Claim 41 also recites a capacitor structure that includes a second capacitor that is disposed adjacent to a first capacitor and that includes s third external terminals that are coupled to corresponding ones of said s second terminals of said first capacitor.

Galvangi et al. does not show, teach or suggest arranging and connecting a first capacitor adjacent to a second capacitor. Rather, Galvangi et al. shows a first capacitor

mounted on top of a second capacitor. There are no external pads shown on sides of the capacitor structure in Galvangi et al. Therefore, adjacent connection was not contemplated.

Applicants note that the rejection in paragraph 14 of the Office Action on page 23 does not expressly include a rejection of Claim 61. However, the body of the rejection at page 33 describes the rejection of Claim 61. In the following discussion, Applicant assumes that Claim 61 was meant to be rejected by the Examiner in view of Galvagni et al. and DuPre.

With respect to Claim 61, in addition to the claim recitations and arguments identified above with respect to Claim 24, Claim 61 also recites a capacitor structure that includes a second capacitor that is disposed abutting and adjacent to a first capacitor and that includes q third external terminals that are coupled to corresponding ones of said s second terminals of said first capacitor.

Galvangi et al. does not show, teach or suggest arranging and connecting a first capacitor in an abutting and adjacent orientation relative to a second capacitor. Rather, Galvangi et al. shows a first capacitor mounted on top of a second capacitor. There are no external pads shown on sides of the capacitor structure in Galvangi et al. Therefore, adjacent connection was not contemplated.

Therefore, Applicants believe that Claims 24, 41 and 61 are allowable over the combination of Galvangi et al. and DuPre et al.

Claims 24, 26-30, 31-32, 34-36, 41-43, 45-51, 53, 59, 61-62, 70, 72-74, 77, and 88 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Li et al. (U.S. Patent No. 6,636,416) in view of Naito et al. (U.S. Patent No. 6,072,687).

Claims 24, 41 and 61 recite a capacitor that includes m electrode plates that are oriented perpendicular to a substrate.

The Examiner admits that Li et al. does not teach any of the recited elements of these Claims other than first and second connected capacitors. As best understood by Applicant, neither Li et al. nor Naito et al. show, teach or suggest a capacitor having m electrode plates that are oriented perpendicular to a substrate. As described above, this relationship increases the real estate required by the capacitor structure.

Therefore, Applicant believes that Claims 24, 41 and 61 are allowable over the combination of Li et al. and Naito et al.

Applicants have thus addressed the rejections of independent Claims 1, 24, 41 and 61. Claims 2-8, 10-17, 23, 25-32, 34-36, 42-51, 53, 58-60, 62-83, 85-90, and 92 and are either directly or indirectly dependent upon Claims 1, 24, 41 and 61 and are therefore allowable for the same reasons.

With respect to Claims 9, 33 and 52, Applicant has rewritten Claim 9, 33 and 52 into independent form. None of the references show, teach or suggest the specific arrangement of a capacitor structure having electrode plates that are oriented perpendicular to the substrate and n or s first external terminals, wherein n or s is 4, a first one and a second one of the n or s first external terminals are arranged in a first row, a third one and a fourth one of the n or s first external terminals are arranged in a second row, the first one of the n or s first external terminals is arranged adjacent the second and fourth ones of the n or s first external terminals and diagonal to the third one of the n or s first external terminals, and the second one of the n or s first external terminals is arranged diagonal to the fourth one of the n or s first external terminals.

Therefore, Claims 9, 33 and 52 are allowable over the prior art of record.

With respect to Claims 18, 37 and 54, Applicant has rewritten Claim 18, 37 and 54 into independent form. None of the references show, teach or suggest connecting a capacitor structure as claimed to an inductor also as claimed.

Therefore, Claims 18, 37 and 54 are allowable over the prior art of record. Claims 19-22, 38-40, and 55-57 are either directly or indirectly dependent upon Claims 18, 37 and 54 and are therefore allowable for the same reasons.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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By: _____
Michael D. Wiggins
Reg. No. 34,754

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. Box 828
Bloomfield Hills, Michigan 48303
(248) 641-1600